

IMPROVED BALL GRID ARRAY PACKAGE AND PROCESS FOR MANUFACTURING SAME

CROSS REFERENCE TO RELATED APPLICATION

[0001] This is a continuation-in-part of applicant's co-pending United States patent application entitled, Improved Ball Grid Array Package and Process for Manufacturing Same, filed August 20, 2003, which is a continuation of co-pending United States patent application No. 10/323,657 entitled, Process For Manufacturing Ball Grid Array Package, filed December 20, 2002, which is a continuation-in-part of United States patent application serial no. 10/197,832 entitled Improved Ball Grid Array Package, filed July 19, 2002. The contents of each of these applications is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates in general to integrated circuit packaging, and in particular to an improved ball grid array package with enhanced thermal characteristics and a unique method of manufacturing the ball grid array package.

BACKGROUND OF THE INVENTION

[0003] High performance integrated circuit (IC) packages are well known in the art. Improvements in IC packages are driven by industry demands for increased thermal and electrical performance and decreased size and cost of manufacture.

[0004] In general, array packaging such as Plastic Ball Grid Array (PBGA) packages provide a high density of interconnects relative to the surface area of the package. However, typical PBGA packages include a convoluted signal path, giving rise to high impedance and an inefficient thermal path which results in low thermal dissipation performance. With increasing package density, the spreading of heat generated by the package is increasingly important.

[0005] Reference is made to Figure 1, which shows an elevation view of a conventional PBGA package indicated generally by the numeral 20. The PBGA package 20 includes a substrate 22 and a semiconductor die 24 attached to the substrate 22 by a die adhesive. Gold wire bonds 26 electrically connect the die 24 to metal traces on the substrate 22. The wire

bonds and die 24 are encapsulated in a molding compound 28. Solder balls 30 are disposed on the bottom surface of the substrate 22 for signal transfer. Because of the absence of a thermal path away from the semiconductor die 24, thermal dissipation in this package is poor.

[0006] Variations to conventional BGA packages have been proposed for the purpose of increasing thermal and electrical performance. One particular variation includes the addition of a metal heat spreader to the package, as shown in Figure 2 which shows an elevation view of a PBGA package 20 of the prior art including the heat spreader, indicated by the numeral 32. In general, the metal heat spreader is fixed to the molded package. This package suffers disadvantages, however, as heat must be dissipated from the semiconductor die 24, through the molding compound 28 and then through the heat spreader 32.

[0007] It is therefore an object of an aspect of the present invention to provide a process for manufacturing a BGA package with a heat spreader that obviates or mitigates at least some of the disadvantages of the prior art.

SUMMARY OF THE INVENTION

[0008] In one aspect, a ball grid array integrated circuit package is manufactured by mounting a semiconductor die, to a first surface of a substrate such that bumps on the semiconductor die are electrically connected to conductive traces of the substrate. At least one collapsible spacer is mounted to at least one of a heat spreader, the semiconductor die and the substrate. The heat spreader is fixed to the at least one of the first surface of the substrate and the semiconductor die such that the at least one collapsible spacer is disposed therebetween. A ball grid array is formed on a second surface of the substrate, bumps of the ball grid array being electrically connected to the conductive traces and the integrated circuit package is singulated.

[0009] In another aspect, a ball grid array integrated circuit package is manufactured by mounting a semiconductor die, to a first surface of a substrate such that bumps on the semiconductor die are electrically connected to conductive traces of the substrate. At least one collapsible spacer is mounted to at least one of a heat spreader, the semiconductor die and the substrate. One of the heat spreader and the substrate is placed in a mold cavity and ; the other of the heat spreader and the substrate is releasably clamped to a die of the mold cavity, such that the collapsible spacer is disposed between the heat spreader and the substrate. A molding compound is molded in the mold, thereby molding the semiconductor die, the substrate, the at

least one collapsible spacer and the heat spreader into the molding compound to provide a molded package. A ball grid array is formed on a second surface of the substrate, bumps of the ball grid array being electrically connected to the conductive traces and the integrated circuit package is singulated.

[0010] In another aspect, there is provided a process for manufacturing a plurality of integrated circuit packages. The process includes mounting a plurality of semiconductor dice to a first surface of a substrate array such that bumps on the semiconductor dice are electrically connected to conductive traces of the substrate. A collapsible spacer array is mounted to one of a heat spreader array and the substrate array. One of the heat spreader array and the substrate array is placed in a mold cavity and the other of the heat spreader array and the substrate array is clamped to a first die of the mold such that the collapsible spacer array is disposed between the heat spreader array and the substrate array. A molding compound is molded in the mold, thereby molding the semiconductor dice, the substrate array, the collapsible spacer array and the heat spreader array into the molding compound to provide an array of molded packages. A plurality of ball grid arrays are formed on a second surface of the substrate array, bumps of the ball grid arrays being electrically connected to the conductive traces, and each integrated circuit package is singulated from the array of molded packages.

[0011] In yet another aspect, there is provided an integrated circuit package. The integrated circuit package includes a substrate having a plurality of conductive traces and a semiconductor die flip-chip mounted to a first surface of the substrate such that bumps of the semiconductor die are electrically connected to the ones of the plurality of conductive traces. A heat spreader is disposed proximal to and spaced from the semiconductor die by at least one collapsible spacer. A molding compound encapsulates the semiconductor die and the collapsible spacer between the substrate and the heat spreader. A ball grid array is disposed on a second surface of the substrate, bumps of the ball grid array being electrically connected to the conductive traces.

[0012] Advantageously, a heat spreader is incorporated into the BGA package during manufacture. The heat spreader is prepared and placed in the mold and is incorporated into the package by molding. An array of heat spreaders is placed in the mold and molded with a substrate array such that a plurality of packages including heat spreaders are manufactured in a single mold shot.

[0013] A thermal path is provided from the semiconductor die, through the collapsible

spacer and to the heat spreader. Also, the heat spreader is effectively pressed against the lower mold die surface during molding, thereby inhibiting mold flash on the outer side of the heat spreader. The incorporation of a deformable material (collapsible spacer) that is stable at molding temperature, provides a compliant layer between the substrate and the heat spreader and the between the semiconductor die and the heat spreader. Thus, the heat spreader is pressed against the lower mold die, maintaining the heat spreader in contact with the lower mold die during molding and reducing mold flash.

[0014] In another aspect, the semiconductor die is bonded to the semiconductor die is attached to the substrate such that pads of the semiconductor die are electrically connected to the conductive traces of the substrate. Thus, wire bonds between the semiconductor die and the substrate are not required in the present embodiment. Advantageously, this arrangement obviates problems associated with electrical impedance in wire bonds.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The invention will be better understood with reference to the following description and to the drawings, in which:

[0016] Figure 1 shows an elevation view of a conventional plastic ball grid array package;

[0017] Figure 2 shows an elevation view of a prior art plastic ball grid array package including a heat spreader;

[0018] Figures 3A to 3J show processing steps for manufacturing a ball grid array package, in accordance with one embodiment of the present invention;

[0019] Figure 4 shows a mold including molding dies and a mold cavity for molding the ball grid array package according to an embodiment of the present invention;

[0020] Figures 5A to 5J show processing steps for manufacturing a ball grid array package, in accordance with another embodiment of the present invention;

[0021] Figures 6A to 6J show processing steps for manufacturing a ball grid array package, in accordance with yet another embodiment of the present invention;

[0022] Figures 7A to 7I show processing steps for manufacturing a ball grid array package, in accordance with another embodiment of the present invention; and

[0023] Figures 8A to 8H show processing steps for manufacturing a ball grid array package, in accordance with still another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0024] Reference is now made to Figures 3A to 3J to describe a process for manufacturing a ball grid array integrated circuit package, referred to herein as a ball grid array package, according to an embodiment of the present invention. To simplify the description, the numerals used previously in describing Figure 1 will be used again after raising the numerals by 100 where parts to be described correspond to parts already described.

[0025] Referring to Figure 3J, the ball grid array package is indicated generally by the numeral 120. The ball grid array package 120 includes a substrate 122 having a plurality of conductive traces and a semiconductor die 124 flip-chip mounted to a first surface of the substrate 122 such that bumps 140 of the semiconductor die 124 are electrically connected to the ones of the plurality of conductive traces. A heat spreader 132 is disposed proximal to and spaced from the semiconductor die 124 by at least one collapsible spacer 136. A ball grid array 130 is disposed on a second surface of the substrate 122, bumps of the ball grid array 130 being electrically connected to the conductive traces.

[0026] The process for manufacturing the ball grid array package 120, according to one embodiment of the present invention, will now be described in more detail. Referring to Figure 3A, the substrate 122 of a BT resin/glass epoxy printed circuit board with conductive traces for signal transfer is shown. A solder mask is disposed on the lower surface of the substrate, with portions of the conductive traces (interconnects) exposed. The substrate 122 is in the form of an array strip for producing a number of BGA units. Three such units are depicted in an array in Figure 3A.

[0027] The singulated semiconductor die 124 including solder bumps 140 on conductive pads of the semiconductor die 124, is flip-chip mounted to an upper surface of the substrate 122 by solder reflow technique. (Figure 3B). As will be appreciated, the semiconductor die 124 is flip-chip mounted such that the solder bumps 140 are mounted to ones of the conductive traces of the substrate 122, thereby electrically connecting the conductive pads of the semiconductor die 124 to the conductive traces of the substrate 122.

[0028] Next, the gap between the semiconductor die 124 and the top surface of the substrate 122 is underfilled with epoxy (Figure 3C).

[0029] The heat spreader 132 is manufactured in the form of an array frame that is compatible with the substrate array 122 (Figure 3D). In the present embodiment the heat spreader is a copper strip that is etched to form the array frame. The array frame includes a number of heat spreaders 132 joined together by partially-etched tie-bars. Three such heat spreaders are depicted in Figure 3D.

[0030] A plurality of collapsible spacers 136 are manufactured in the form of an array that is compatible with the substrate array 122 and the heat spreader 132 (Figure 3E). The collapsible spacers 136 are comprised of a solder preform of a plurality of substantially spherical balls connected together by tie bars. The collapsible spacers 136 are mounted to the substrate 122 using epoxy. It will be appreciated that some of the collapsible spacers 136 are mounted directly on the substrate 122 and other collapsible spacers 136 are mounted to corresponding semiconductor dice 124 (Figure 3F).

[0031] The heat spreader 132, in the array format, is placed in the bottom of a mold die cavity, on the lower surface of the mold. Features of the mold cavity and the frame are designed such that the heat spreader 132 aligns with the substrate 122 in the die cavity. The substrate array strip 122 is clamped to a surface of an upper mold die, in the mold cavity such that the semiconductor die 124 and the collapsible spacers 136 protrude from the substrate 22 into the mold cavity. The collapsible spacers 136, in the array format, are thus disposed between the heat spreader 132 and the substrate 122 (Figure 3G). A suitable mold including the molding dies and mold cavity is shown in Figure 4.

[0032] Molding using a molding compound 128 in the mold die cavity follows. During molding, the collapsible spacers 136 are compressed between the substrate 122 and the heat spreader 132 and between the semiconductor die 124 and the heat spreader 132, causing deformation of the collapsible spacers 136 (Figure 3H). The heat spreader 132 is thereby pressed against the lower surface of the mold in the mold die cavity. The molding compound 128 encapsulates the semiconductor die 124, and the collapsible spacers 136 between the heat spreader 132 and the substrate 122, and joins the heat spreader 132 to the remainder of the package 120.

[0033] After removing the package 120 from the mold, the solder balls 130, also referred to

as solder bumps, in the form of a ball grid array, are formed on the lower surface of the substrate 122 by conventional positioning (Figure 3I). To attach the solder balls 130, a flux is added to the balls prior to placement and, after placement the solder balls 130 are reflowed using known reflow techniques. The solder balls 130 are thereby connected to the conductive traces of the substrate 122 and through the solder bumps 140 of the semiconductor die 124 to the semiconductor die 124. The solder balls 130 provide signal and power connections as well as ground connections for the semiconductor die 124.

[0034] Singulation of the individual BGA unit from the array strip is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 3J. Thus, the individual BGA package is isolated from the strip.

[0035] Reference is now made to Figures 5A to 5J to describe a process for manufacturing the ball grid array package 120, in accordance with another embodiment of the present invention. Figures 5A to 5E are similar to Figures 3A to 3E and therefore need not be further described herein. In Figure 5F, however, the collapsible spacers 136 are mounted to the heat spreader 132, rather than the substrate 122. The heat spreader 132, in the array format, is then placed in the bottom of the die cavity, on the lower surface of the mold such that the collapsible spacers 136 protrude into the mold cavity. Features of the mold cavity and the frame are designed such that the heat spreader 132 aligns with the substrate 122 in the die cavity. The substrate array strip 122 is clamped to a surface of an upper mold die, in the mold cavity such that the semiconductor die 124 protrudes from the substrate 122 into the mold cavity. The collapsible spacers 136, in the array format, are thus disposed between the heat spreader 132 and the substrate 122 and between the heat spreader 132 and the semiconductor die 124 (Figure 5G). Figures 5H to 5J are similar to Figures 3I to 3J and therefore need not be further described herein.

[0036] Referring now to Figures 6A to 6J to describe a process for manufacturing the ball grid array package 120, in accordance with yet another embodiment of the present invention, Figures 6A to 6F are similar to Figures 3A to 3F and therefore need not be further described herein. In Figure 6G, however, the substrate 122 is placed in the bottom of the mold die cavity, on the lower surface of the mold. Features of the mold cavity and the frame are designed such that the substrate 122 aligns with the heat spreader 132. The semiconductor die 124 and the collapsible spacers 136 protrude from the substrate 122. The heat spreader 132 is clamped to the surface of the upper mold die in the mold cavity. The collapsible spacers 136, in the array

format, are thus disposed between the heat spreader 132 and the substrate 122.

[0037] Molding using a molding compound 128 in the mold die cavity follows. During molding, the collapsible spacers 136 are compressed between the substrate 122 and the heat spreader 132 and between the semiconductor die 124 and the heat spreader 132, causing deformation of the collapsible spacers 136 (Figure 6H). The substrate 122 is thereby pressed against the lower surface of the mold in the mold die cavity. The molding compound 128 encapsulates the semiconductor die 124, and the collapsible spacers 136 between the heat spreader 132 and the substrate 122, and joins the heat spreader 132 to the remainder of the package 120.

[0038] Figures 6 I and 6J are similar to Figures 3I and 3J and therefore need not be further described herein.

[0039] Reference is now made to Figures 7A to 7H to describe a process for manufacturing a ball grid array package 120 in accordance with still another embodiment. Figures 7A to 7C are similar to Figures 3A to 3C and therefore need not be further described herein. In Figure 7D, however, individual heat spreaders 132 are manufactured. In the present embodiment, each heat spreader 132 is copper.

[0040] Figures 7E and 7F are similar to Figures 3E and 3F and therefore need not be further described herein.

[0041] In Figure 7G, each heat spreader 132 is individually placed on collapsible spacers 136 on a respective substrate 122 and semiconductor die 124, followed by reflow of the solder preform collapsible spacers 136. Thus, each heat spreader 136 is fixed to both the substrate 122 and the respective semiconductor die 124. In an alternative embodiment, the collapsible spacers 136 are made of a thermoplastic material with low modulus, such as polycarbonate. In this embodiment, each heat spreader 132 is individually placed on a collapsible spacer 136 on a respective substrate 122 and a semiconductor die 124, followed by thermally setting the collapsible spacers 136. In each case, each heat spreader 136 is fixed to both the substrate 122 and the semiconductor die 124 by the collapsible spacers 136.

[0042] After fixing the heat spreader 136 to the substrate 122 and the semiconductor die 124, the solder balls 130, in the form of a ball grid array, are formed on the lower surface of the substrate 122 by conventional positioning (Figure 7G). To attach the solder balls 130, a flux is added to the balls prior to placement and, after placement the solder balls 130 are reflowed

using known reflow techniques. The solder balls 130 are thereby connected to the conductive traces of the substrate 122 and through the solder bumps 140 of the semiconductor die 124 to the semiconductor die 124. The solder balls 130 provide signal and power connections as well as ground connections for the semiconductor die 124.

[0043] Singulation of the individual BGA unit from the array strip is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 7H. Thus, the individual BGA package is isolated from the strip.

[0044] Reference is now made to Figures 8A to 8H to describe a process for manufacturing a ball grid array package 120 in accordance with still another embodiment. Figures 8A to 8C are similar to Figures 5A to 5F and therefore need not be further described herein. In Figure 8D, however, individual heat spreaders 132 are manufactured.

[0045] Next, collapsible spacers 136 are mounted to the individual heat spreaders 136 as shown in Figure 8E, using, for example, epoxy. Each heat spreader 136, including the collapsible spacers 136, is placed on and mounted to the substrate 122 and a respective semiconductor die 124, as shown in Figure 8F. Reflow of the solder preform collapsible spacers 136 follows. Thus, each heat spreader 136 is fixed to both the substrate 122 and the respective semiconductor die 124. In an alternative embodiment, the collapsible spacers are made of a thermoplastic material with low modulus, such as polycarbonate. In this embodiment, the heat spreader 132 is placed on the substrate 122, followed by thermally setting the collapsible spacer 136. In each case, the heat spreader 136 is fixed to both the substrate 122 and the semiconductor die 124 by the collapsible spacers.

[0046] After fixing the heat spreaders 136 to the substrate 122 and the semiconductor dice 124, the solder balls 130, in the form of a ball grid array, are formed on the lower surface of the substrate 122 by conventional positioning (Figure 8G). To attach the solder balls 130, a flux is added to the balls prior to placement and, after placement the solder balls 130 are reflowed using known reflow techniques. The solder balls 130 are thereby connected to the conductive traces of the substrate 122 and through the solder bumps 140 of the semiconductor die 124 to the semiconductor die 124. The solder balls 130 provide signal and power connections as well as ground connections for the semiconductor die 124.

[0047] Singulation of the individual BGA unit from the array strip is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 8H. Thus, the

individual BGA package is isolated from the strip.

[0048] Alternative embodiments and variations are possible. In one alternative embodiment, the collapsible spacers 136 are individually placed on the substrate 122 and die adapter 134 or on the heat spreader 132, rather than being manufactured in the form of an array. The collapsible spacers 136 are placed in the appropriate position with pre-dispensed flux using pick and place technology, followed by solder reflow. In still another alternative embodiment, epoxy is pre-applied to the substrate 122 and the die adapter 134 or on the heat spreader 132, the collapsible spacers 136 are placed using pick and place technology and the epoxy is cured.

[0049] For example, rather than placing the heat spreader in the bottom of the mold cavity and clamping the substrate to the top mold die, the substrate can be placed in the bottom of the mold cavity and the heat spreader clamped to the top of the mold die. Rather than etching a copper strip to prepare the array frame of heat spreaders 132, the frame can be manufactured by metal stamping. Also, the heat spreader is not limited to copper as other suitable heat spreader materials are possible and will occur to those skilled in the art. In the above-described embodiments, the collapsible spacers are mounted to the substrate or the heat spreader using epoxy, however other means for mounting the collapsible spacers are possible. For example, the collapsible spacers can be mounted using solder reflow technique. Also, the collapsible spacers are not limited to solder preform as other suitable materials can be employed, including for example, low modulus conductive polymer such as silicone or a thermoplastic material with low modulus such as polycarbonate. Still other embodiments and variations may occur to those of skill in the art. All such embodiments and variations are believed to be within the scope and sphere of the present invention.